REMARKS

Claims 1-21 and 39-47 are all the claims presently pending in the application. Claims 41-47 are canceled above.

Claims 1-18 and 39-40 stand rejected under §112, second paragraph. Claim 19 stands rejected under 35 USC §102(e) as anticipated by US Patent 6,218,274 to Komatsu. Claims 41-47 stand rejected under 35 USC §102(e) as anticipated by US Patent 6,238,737 to Chan et al. Applicants respectfully traverse these rejections, as discussed below.

It is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

As described and claimed, for example, by claim 1, the present invention is directed to a method of forming a semiconductor substrate, including forming a metal back-gate over a first substrate. A passivation layer is formed on the metal back-gate to prevent the metal back-gate from reacting with radical species.

An intermediate gluing layer is provided on the passivation layer to enhance adhesion between the metal back-gate and a handle substrate. A low temperature oxide (LTO) layer is deposited on the intermediate gluing layer, and the handle substrate is then bonded to the LTO layer.

With the above and other unique unobvious aspects of the present invention, making substrates for double-gate devices with a metal back-gate can be performed including using wafer bonding and despite after the room-temperature joining step, a thermal treatment at 1100°C is used to enhance the bonding strength.

That is, even with chemical and physical incompatibility of layers, the stacked layers are not likely to disintegrate during the high temperature bonding anneal, and delamination will not occur at the interfaces.

Thus, the present invention resolves the above-mentioned and other problems of delamination between, for example, W and low temperature oxide (LTO) during bonding

anneal by improving the adhesion between these two incompatible materials with several innovative processes.

None of the cited references, either alone or in combination, teaches or suggests such a combination of features.

II. THE 35 USC §112, FIRST PARAGRAPH, REJECTION

Claims 1-18 and 29-40 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Applicants believe that the above claim clarifications properly address the Examiner's concerns and the Examiner is requested to reconsider and withdraw this rejection.

However, Applicants wish to respond on the record that the Examiner's definition of "on" (e.g., "over and in contact with") is only one of a plurality of possible meanings for this word and that it is unreasonable to declare that this single, very limited, definition is generic, let alone that it is the only definition that one of ordinary skill in the art would apply.

The meaning of "on" depends entirely upon the context of its use. More specifically, it is pointed out that this word "on", when used in microelectronics as a preposition, is just as frequently understood as meaning "so as to be or remain supported by or suspended from". Additionally, Applicants submit that there is no inherent implication of direct contact, as the expression "the book on the table" is considered correctly used even though the book actually contacts a table cloth, rather than the table surface directly.

Therefore, although Applicants do not dispute that the Examiner's preferred definition of "on" is correct in some circumstances, it is not universally correct and cannot be reasonably stated as being the only meaning that one of ordinary skill in the art would attribute in all contexts.

III. THE PRIOR ART REJECTIONS

Relative to the rejection for claim 19, the Examiner alleges that Komatsu teaches the present invention as defined by that claim. As best understood, the Examiner relies upon the various figures Komatsu, beginning at Figure 17, and considers that WSi_x layer 41

corresponds to the refractory metal layer of claim 19 and that Si_3N_4 film 43 corresponds to the passivation layer of the claim.

However, this interpretation fails to honor the plain meaning of the claim language, in which it is described that the passivation layer results from steps including the desorbing of the native oxide on the metal in order to be able to form the passivation layer, having the form metal-Si-N, on the bare metal. Thus, the simple Si_3N_4 film 43 would fail to qualify in both composition and process steps.

In contrast, the present invention defined by this claim allows a very thin (e.g., monolayer) of metal-Si with the bare metal surface, with subsequent steps completing the metal-Si-N passivation layer.

Hence, turning to the clear language of the claim, there is no teaching or suggestion in Komatsu of:"... forming a passivation layer, having a form metal-Si-N, on said refractory metal by initially desorbing a native oxide thereon to be able to form said passivation layer on a bare surface of said metal", as required by claim 19.

Relative to the rejection for claims 41-47, the Examiner alleges that Chan et al. teaches the methods of these claims. However, although there are arguably similarities, the present invention includes, in the formation of the passivation layer, an initial step in which the native oxide of the metal layer is desorbed, using a high vacuum for about five minutes, as described at lines 10-12 on page 7 of the specification. Chan fails to teach or reasonably suggest this initial step in the passivation layer formation.

Hence, turning to the clear language of the claims, there is no teaching or suggestion in Chan of: "... desorbing a native oxide of said metal ...", as required in independent claims 41, 43, and 45. Therefore, claims 41-47 are clearly patentable over Chan.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too, even in combination with Komatsu or Chan, fails to teach or suggest the claimed invention.

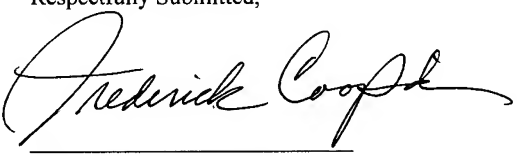
IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-21 and 39-47, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0510.

Respectfully Submitted,



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